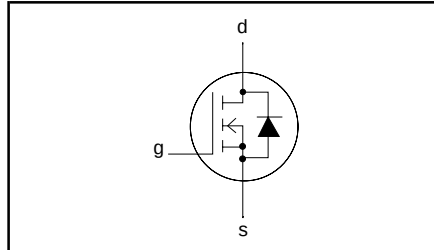


SiliconMAX**N-channel TrenchMOS™ transistor****PSMN020-150W****FEATURES**

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Low thermal resistance

SYMBOL**QUICK REFERENCE DATA**

$$V_{DSS} = 150 \text{ V}$$

$$I_D = 73 \text{ A}$$

$$R_{DS(ON)} \leq 20 \text{ m}\Omega$$

GENERAL DESCRIPTION

SiliconMAX products use the latest Philips Trench technology to achieve the lowest possible on-state resistance in each package at each voltage rating.

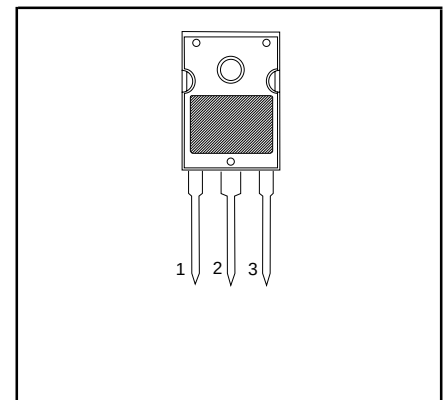
Applications:-

- d.c. to d.c. converters
- switched mode power supplies

The PSMN020-150W is supplied in the SOT429 (TO247) conventional leaded package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

SOT429 (TO247)**LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25^\circ\text{C}$ to 175°C	-	150	V
V_{DGR}	Drain-gate voltage	$T_j = 25^\circ\text{C}$ to 175°C ; $R_{GS} = 20 \text{ k}\Omega$	-	150	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Continuous drain current	$T_{mb} = 25^\circ\text{C}$	-	73	A
		$T_{mb} = 100^\circ\text{C}$	-	51	A
I_{DM}	Pulsed drain current	$T_{mb} = 25^\circ\text{C}$	-	290	A
P_D	Total power dissipation	$T_{mb} = 25^\circ\text{C}$	-	300	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	$^\circ\text{C}$

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, $I_{AS} = 73 \text{ A}$; $t_p = 100 \mu\text{s}$; T_j prior to avalanche = 25°C ; $V_{DD} \leq 25 \text{ V}$; $R_{GS} = 50 \Omega$; $V_{GS} = 5 \text{ V}$; refer to fig:15	-	707	mJ
I_{AS}	Non-repetitive avalanche current		-	73	A



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THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	in free air	-	0.5	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient		45	-	K/W

ELECTRICAL CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 0.25\text{ mA}$; $T_j = -55^\circ\text{C}$	150	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1\text{ mA}$; $T_j = -55^\circ\text{C}$	134	-	-	V
		$T_j = 175^\circ\text{C}$	2.0	3.0	4.0	V
		$T_j = -55^\circ\text{C}$	1.0	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 175^\circ\text{C}$	-	-	6	V
			-	12	20	mΩ
			-	-	56	mΩ
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 10\text{ V}$; $V_{DS} = 0\text{ V}$	-	2	100	nA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 150\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 175^\circ\text{C}$	-	0.05	10	μA
			-	-	500	μA
$Q_{g(tot)}$	Total gate charge	$I_D = 73\text{ A}$; $V_{DD} = 120\text{ V}$; $V_{GS} = 10\text{ V}$	-	227	-	nC
Q_{gs}	Gate-source charge		-	46	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	91	-	nC
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 75\text{ V}$; $R_D = 2.7\ \Omega$; $V_{GS} = 10\text{ V}$; $R_G = 5.6\ \Omega$	-	34	-	ns
t_r	Turn-on rise time	Resistive load	-	79	-	ns
$t_{d\ off}$	Turn-off delay time		-	233	-	ns
t_f	Turn-off fall time		-	101	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$	-	9537	-	pF
C_{oss}	Output capacitance		-	854	-	pF
C_{rss}	Feedback capacitance		-	380	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	73	A
I_{SM}	Pulsed source current (body diode)		-	-	290	A
V_{SD}	Diode forward voltage	$I_F = 25\text{ A}$; $V_{GS} = 0\text{ V}$	-	0.85	1.2	V
		$I_F = 75\text{ A}$; $V_{GS} = 0\text{ V}$	-	1.1	-	V
t_{rr}	Reverse recovery time	$I_F = 20\text{ A}$; $-dI_F/dt = 100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_R = 30\text{ V}$	-	127	-	ns
Q_{rr}	Reverse recovery charge		-	1.0	-	μC

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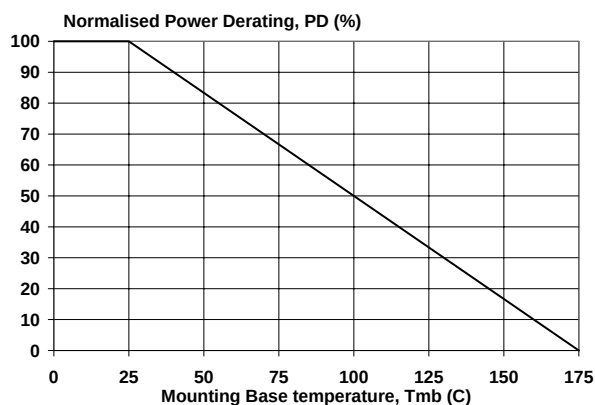


Fig.1. Normalised power dissipation.
 $PD\% = 100 \cdot P_D / P_{D\ 25^\circ\text{C}} = f(T_{mb})$

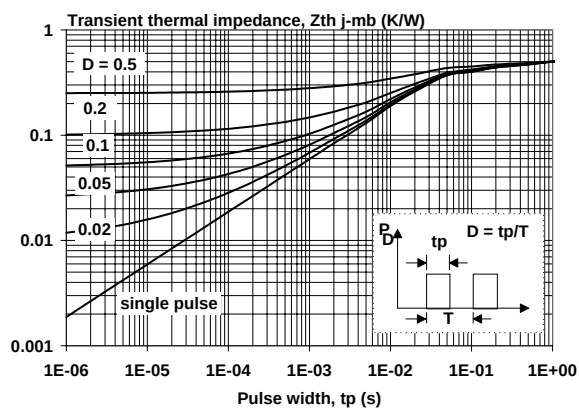


Fig.4. Transient thermal impedance.
 $Z_{th\ j-mb} = f(t)$; parameter $D = t_p/T$

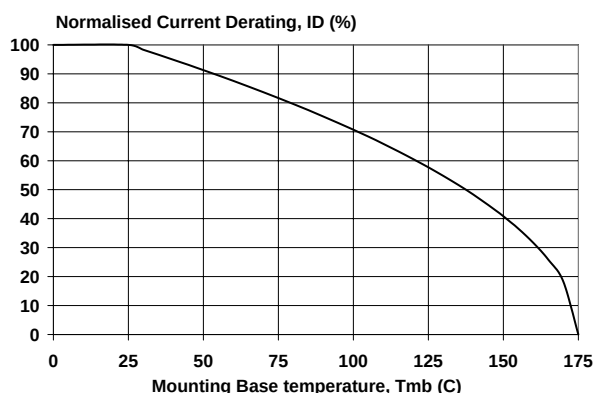


Fig.2. Normalised continuous drain current.
 $ID\% = 100 \cdot I_D / I_{D\ 25^\circ\text{C}} = f(T_{mb})$; $V_{GS} \geq 10\text{ V}$

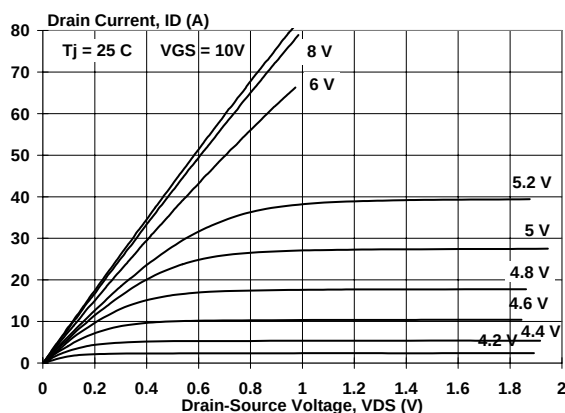


Fig.5. Typical output characteristics, $T_j = 25^\circ\text{C}$.
 $I_D = f(V_{DS})$

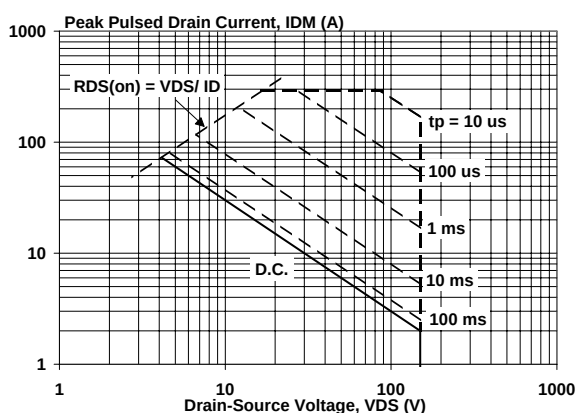


Fig.3. Safe operating area
 I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

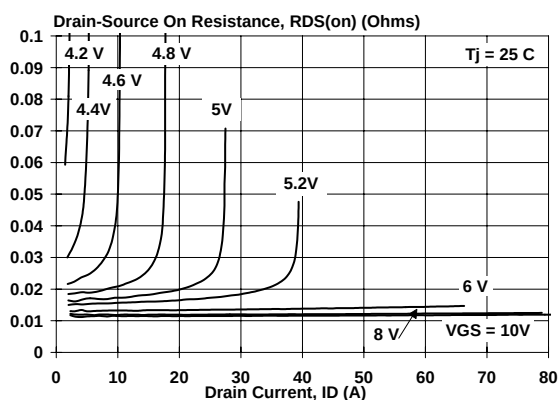


Fig.6. Typical on-state resistance, $T_j = 25^\circ\text{C}$.
 $R_{DS(ON)} = f(I_D)$

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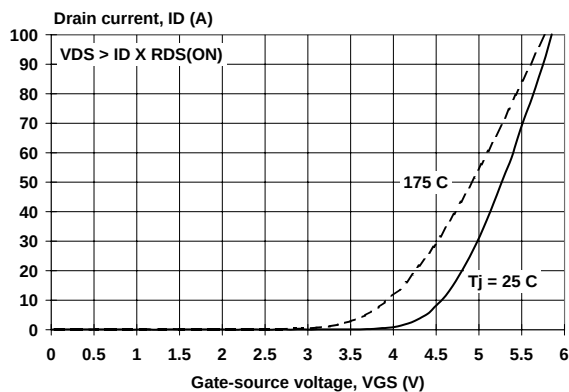


Fig. 7. Typical transfer characteristics.
 $I_D = f(V_{GS})$

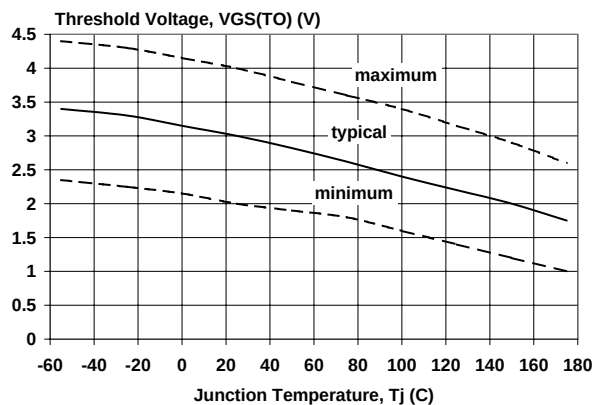


Fig. 10. Gate threshold voltage.
 $V_{GS(T0)} = f(T_j)$; conditions: $I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

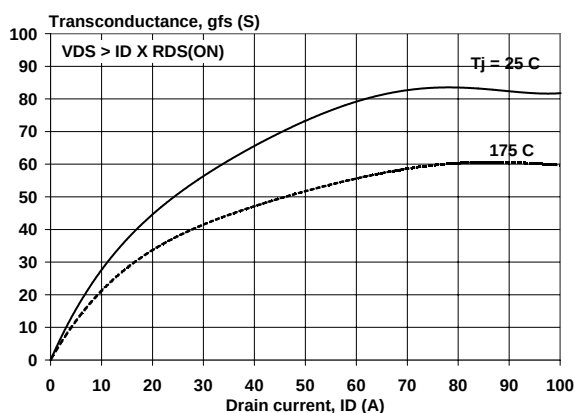


Fig. 8. Typical transconductance, $T_j = 25 \text{ °C}$.
 $g_{fs} = f(I_D)$

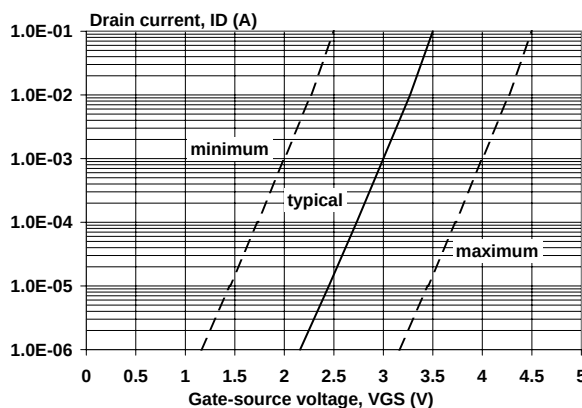


Fig. 11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25 \text{ °C}$

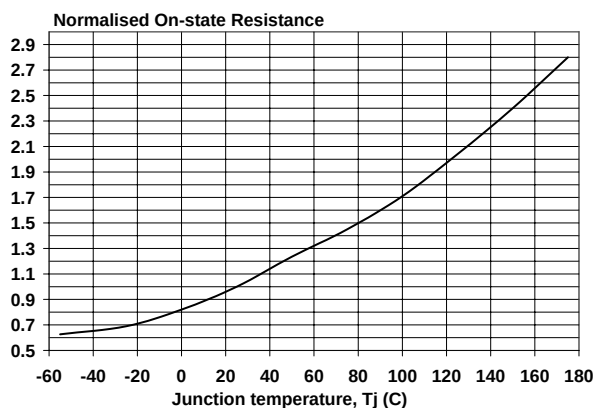


Fig. 9. Normalised drain-source on-state resistance.
 $R_{DS(ON)}/R_{DS(ON)25 \text{ °C}} = f(T_j)$

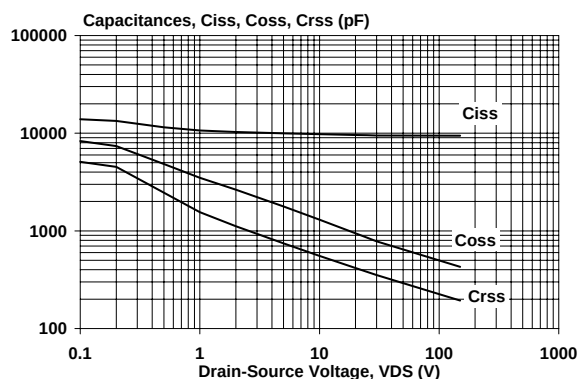


Fig. 12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

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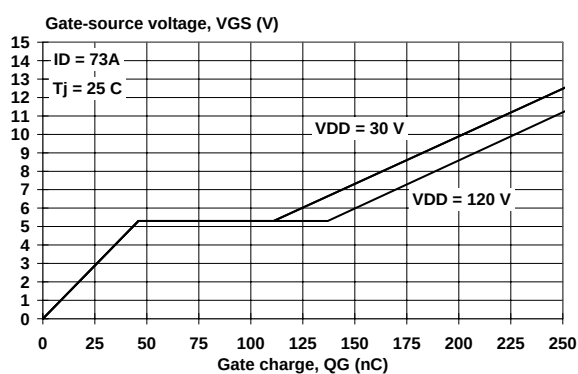


Fig.13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$

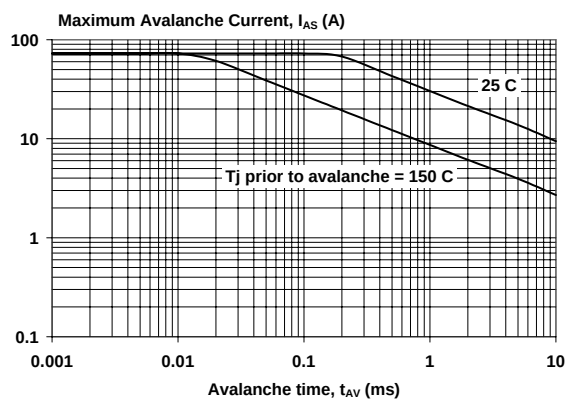


Fig.15. Maximum permissible non-repetitive avalanche current (I_{AS}) versus avalanche time (t_{AV}); unclamped inductive load

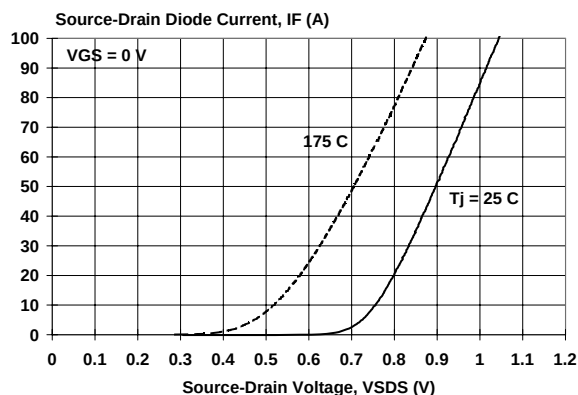


Fig.14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

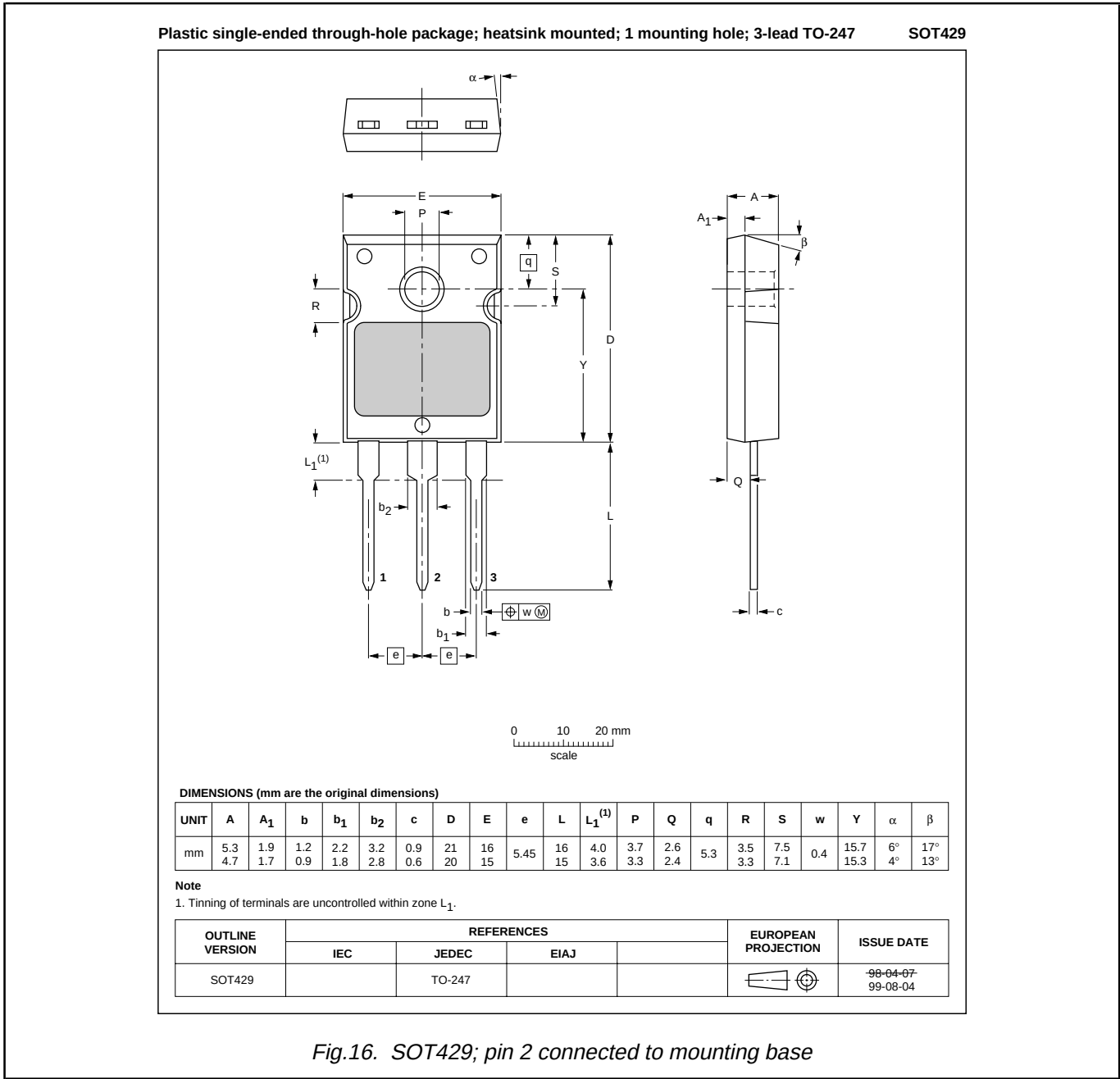
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MECHANICAL DATA



Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT429 envelope.
3. Epoxy meets UL94 V0 at 1/8".



N-channel TrenchMOS™ transistor

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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